Cont'd B1

a select-gate having a portion between the first and second floating gates, the select-gate also extending over at least a portion of each of the two floating gates and extending across the entire length of each of the first and second junctions, and the select gate being separated from the first and second floating gates only by an insulating layer.

28. (Twice Amended) A memory array comprising:

a plurality of cells arranged to form rows and columns of cells, each cell comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

first and second non-contiguous floating gates, the first floating gate extending over a first portion of the channel region and over a portion of the first junction, and the second floating gate extending over a second portion of the channel region and over a portion of the second junction;

B2

a select-gate extending over the two floating gates and extending across the entire length of each of the first and second junctions, the select-gate having a portion between the first and second floating gates, the portion of the select-gate extending over a third portion of the channel region between the first and second channel portions, wherein the first, second, and third portions of the channel region do not overlap and together form the entire channel region;

an inter-polysilicon dielectric layer insulating the first and second floating gates from the select-gate, the select gate being separated from the first and second floating gates only by said inter-polysilicon dielectric layer; and